-CPU II-

Technical description

This unit, with the Z80 microprocessor CPU, controls the entire receiver program sequence. See block diagram CPU II for a list of the individual circuits.

Voltage monitoring and Watchdog

The voltage monitoring circuit consists of the ICs B and D, transistors T 3 and T 4 and the other associated components. The voltage monitored is the +5 V supply, which is fed for this purpose direct from the power supply output to pin b 21 of the circuit. The reference voltage is generated by D 1 and applied to operational amplifier IC - D. The response point of the monitoring circuit is set to 4.81 V with R 3. If the voltage falls below this level, the output of IC - D goes HIGH and an NMI signal originates via IC - B and T 3. After the time lag determined by R 9 and C 6, the RESET signal is also activated via T 4. On switch-on, if the response point is exceeded, the opposite process takes place, the RESET signal being cancelled only after the NMI signal. C 5 and R 8, together with the IC - B, facilitate reliable switchover of output 3 of IC - B on switch-on, thereby preventing oscillation.

The Watchdog circuit comprises IC - C and IC - A. IC - C is a counter chip supplied with the CPU clock pulse via pin 9, so that it counts up. The counter is activated via pin 2 and IC - A is reset if NMI is activated by the voltage monitor or if a reset pulse is generated via decoder IC - Y by the current program. If the program is interrupted for instance by an interference pulse, these reset pulses do not occur and the counter will continue to count until its output Q 24 (pin 1) switches over. This triggers a RESET pulse via IC - A and C 7 and R 11, thereby restarting the CPU via IC - B, T 3 and T 4.

Wait pulse generator

The wait pulse generator comprises two flipflops (IC - F) synchronized with the CPU clock pulse (pins 3 and 11). If an MRQ signal occurs on pin 2, a WAIT signal is generated for the following clock cycle. This makes it possible to use also slower memory chips.

CPU

IC-G is the Z80 CPU which controls and monitors all operating sequences in the RX 1001 M / RX 5001 control unit. The signals NMI and RESET have already been discussed, they ensure a defined program start or interruption. The WAIT signal has also been explained. The address bus A 0 to A 15 is used by the CPU to point to individual storage locations or I/0 chips. The MRQ signal is activated upon memory accesses and the signal IORQ is active on access to I/0 chips. The data direction is determined in each case by the signals RD for READ operations and WR for WRITE operations.

-CPU II-

The system clock pulse is fed to the CPU via pin 6. The bidirectional data bus D 0 to D 7 transfers data between the CPU and the memories and input-output chips. The INT input is used by the peripherals for interrupt requests to the CPU if an interrupt-controlled function is to be performed (e.g., alarm or keyboard entry). The CPU shows by activation of output M 1 that it is executing the first machine cycle of a new instruction. This signal synchronizes the PIOs with the CPU. It is also logically combined with RESET, as an M 1 signal without simultaneous activation of RD or IORQ must be generated for resetting of the PIO circuit.

Clock generator
The clock oscillator comprises Q 1, IC - E, C 8 and R 22 and R 23. The frequency generated is divided by 4 in IC - L and is then 2.4576 MHz. These clock pulses are fed to the CPU, the PIOs, the baud rate generator, the USART, the WAIT pulse generator and the Watchdog.

Baud rate generator
The programmable divider IC - M is supplied with the clock pulse and generates at its output pin 10, 16 times the frequency of the baud rate set on S1. This frequency is fed to the USART as send and receive clock.

Baud rate settings on switch S1:

Baud	S1.1	S1.2	S1.3	S1.4
50	ON	ON	OFF	ON
75	ON	ON	OFF	OFF
110	OFF	OFF	OFF	OFF
134,5	ON	OFF	ON	ON
150	OFF	OFF	OFF	ON
200	ON	OFF	ON	OFF
300	OFF	OFF	ON	OFF
600	ON	OFF	OFF	ON
1200	OFF	ON	OFF	OFF
1800	OFF	ON	OFF	ON
2400	ON	OFF	OFF	OFF
2400	OFF	OFF	ON	ON
4800	OFF	ON	ON	OFF
9600	OFF	ON	ON	ON

Bus drivers
To ensure that the bus connections of the CPU are not overloaded almost all the other units are connected to the CPU via bus drivers. These are IC - H and IC - J for the address bus and IC - K for the monitoring bus. These drivers are constantly selected and operate unidirectionally - i.e., only from the CPU to the connected circuit.

-CPU II-

The driver for the data bus IC - P, on the other hand, operates bidirectionally, as data must be transmitted in both directions, and it is activated only upon memory access operations by the MRQ signal. The data direction of this driver is controlled by RD. The I/O chips are connected direct to the data bus of the CPU to permit the use of Z 80 interrupt mode 2, in which the CPU reads an interrupt vector from the peripheral which has triggered the interrupt. However, this process takes place without activation of the RD line, so that any interconnected bus driver would cause this vector not to be read by the CPU. The data bus driver is in a high-resistance condition upon access operations to the I/O chips.

EPROMs
The IC - N, IC - O chips and possibly also IC - R contain the program whereby the CPU can control and monitor the processes in the equipment. Permanent data are also stored here. The relevant chip is addressed via the CS inputs pins 20 and 22, the address inputs selecting the individual storage location. The content of this storage location is then placed on the data bus and read by the CPU.

RAM with write protection
Circuit IC - I is a static CMOS-RAM, in which the CPU deposits or temporarily stores variable data. When the receiver is switched off, this circuit is powered by the built-in storage battery, so that the stored data is retained and the former operating condition can be restored when the receiver is switched on again. An individual storage location is accessed in the same way as the EPROMs. However, the WR line is also connected to the RAM via pin 27 so that data can also be written into the memory.

A further RAM, IC - S, can also be used if required. Transistors T 1, T 2 and T 5 constitute the write protection for the RAMs when the receiver is switched off or if the power fails. The RESET signal is applied via series resistors to the base connections. If this signal is activated (i.e., LOW) the CS and WR inputs of the RAMs are disconnected by the transistors and kept at HIGH level via R 16, R 24 and R 30. This ensures that no spurious write operations can be initiated and that the data in the RAM is safely retained.

-CPU II-

Decoder for memory Chips
IC - Y selects whichever chip is required by the CPU for storage access operations. The decoder is activated by the MRQ signal via pins 4 and 5 and then switches the output specified by address lines A 15, A 14 and A 13 to LOW level for selection of the connected memory chip. This results in the following address areas:

A 15	A 14	A 13	Address area	Chip	
0	0	0	0000H-1FFFH	EPROM 1	IC - N
0	0	1	2000H-3FFFH	EPROM 2	IC - O
0	1	0	4000H-5FFFH	EPROM 3	IC - R
0	1	1	6000H-7FFFH	Spare RAM	IC - S
1	0	0	8000H-9FFFH	C4 Dec.1	
1	0	1	A000H-BFFFH	CS 6 (Watchdog Trigger)	
1	1	0	C000H-DFFFH	CS 5	
1	1	1	E000H-FFFFH	RAM	IC - T

Further external storage locations are accessed via the signals CS 5, CS 6 and CS Dec. 1.

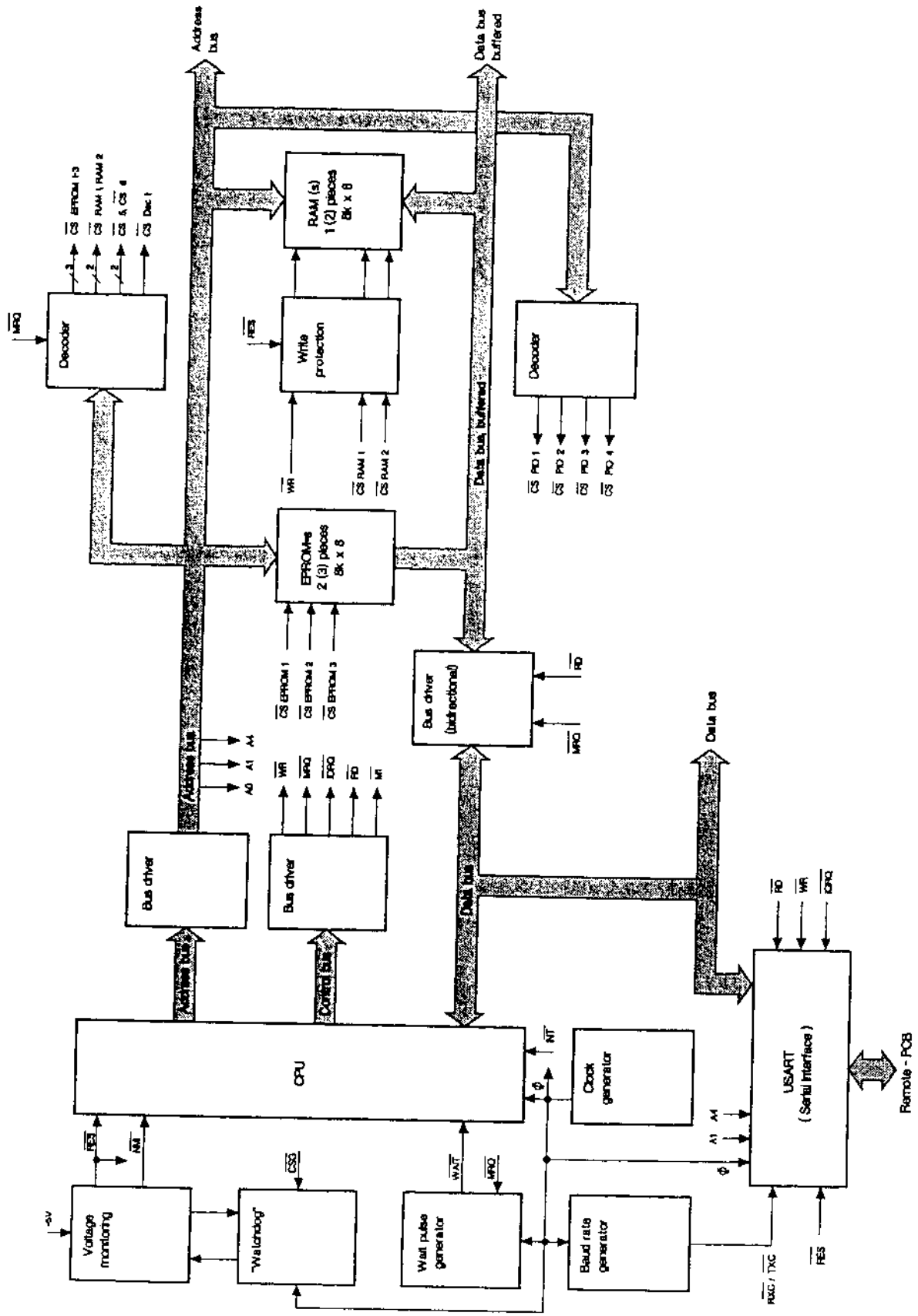
Decoder for input/output chips
Decoder IC - X is activated via pin 1 from address line A 5 and selects a PIO circuit according to the states of lines A 2 and A 3. Since IC - X is controlled only by address lines, its outputs will also generate CS signals on memory access operations. However, these do not matter, as the PIOs also evaluate the IORQ signal for activation.

Serial interface (USART)
IC - V is used for operation of the RS-232 interface. The chip receives the clock pulse via pin 20 and the send-and-receive clock from the baud rate generator via pins 9 and 25. The send-and-receive clock is divided internally by 16 and then forms the baud rate for serial data transmission.

The RESET signal is supplied via pin 21. The CPU is connected to the USART via the data bus D 0 to D 7. The chip is selected for this purpose via CS (pin 11) in combination with RD (pin 13) or WR (pin 10). The read or write signals for IC - V are obtained from the CPU signals by a combination of IORQ, with RD or WR by means of IC - W. CS is connected directly to address line A4, which must therefore be kept at HIGH level for access operations to other I/O chips. The address line is connected directly to input C/D and therefore determines whether data or commands or status information is transmitted over the data bus.

Data is transmitted serially over lines RXD (receive data) and TXD (transmit data). The USART indicates via line RXR that a complete character can be read in serial form. Conversely, an indication is given via TXR that the CPU can write a new character into the chip for serial transmission. When the last character has been completely transmitted, the USART activates the signal TXE. The remaining signals are for modem control: RTS is the request to send, which must be acknowledged by clear to send CTS. The interface signals to the modem that it is ready for operation by DTR (data terminal ready) and the modem activates the DSR (data set ready) line when it is ready for operation.

-CPU II-



Blockdiagram - CPU II

-CPU II-

Test and alignment instrucions

Required: Circuit diagram CPU II - Hagenuk Drawing No. 97 Sa B 2.155.35
DVM, 2-channel oscilloscope, power supply

Test configuration: The PCB is removed and reconnected to the receiver using the extender PCB (service adaptor). Disconnect the 5 V power supply and feed in +5 V externally.

Testing the voltage and current consumption

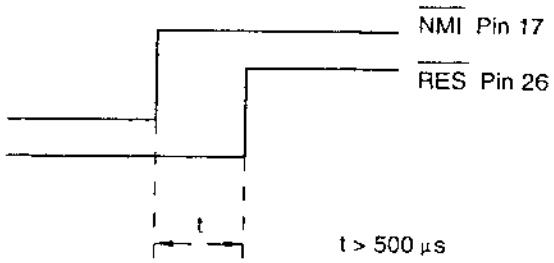
Set external power supply to 5.0 V ± 0.1 V and measure current consumption: specified value 310 mA ± 31 mA.

Testing the voltage monitor circuit

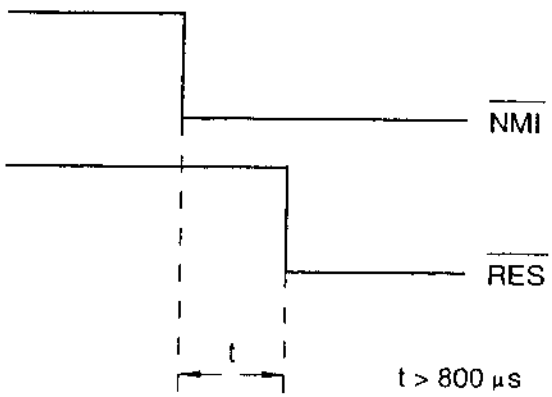
Reduce supply voltage to 4.810 V. Turn potentiometer R 3 fully counterclockwise. Connect a DVM to MP 8. Turn R 3 clockwise.
Test values:
The voltage on MP 8 must be "definitely" LOW.
Then reduce the supply voltage and increase it again.
Test values:
LOW signal on MP 8 at 4.810 V.

-CPU II-

Testing the POWER ON/POWER DOWN circuit
Connect two-channel oscilloscope, channel 1 to IC - G pin 17 and channel 2 to pin 26. Triggering is by the rising edge of the NMI signal. Switch on receiver.
Test values:



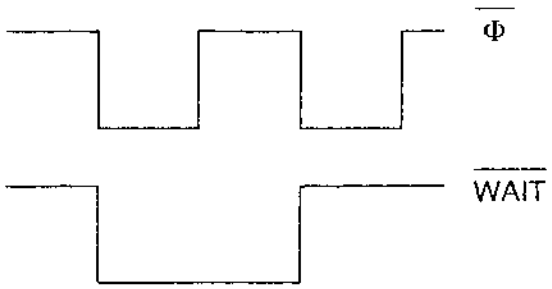
Set triggering to trailing edge of NMI signal.
Interrupt the +5 V power supply.
Test values:



Measurement of CPU clock frequency
Connect oscilloscope to IC - G pin 6. (Ø signal)
Test values:
f = 2.5 MHz.

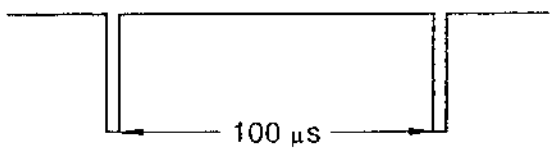
-CPU II-

Measurement of WAIT signal
Connect oscilloscope to IC - G pin 24. (WAIT signal)
Test values:



NOTE
A special test E-PROM is used for further testing of the CPU board.
Remove normal E-PROM set and insert test E-Prom in socket (ICN)

Measure various signals on the CPU board. The test EPROM contains a program which generates all the memory signals. In the subsequent measurement there must be pulses at the measurement points. The pulse form and sequence varies. In the logical "LOW" status the pulses must have a voltage of 0.8 V and in the "HIGH" status a voltage of 2.4 V.
Measure at Pin 20 of IC N, O, R, S, T.
Required: Needle pulses to "LOW", time elapse between the pulses around 100 us.



Measure pulse at Pin 4, 5, 6, 7 IC X.
Required: Pulses

Measure pulses at Pin 9, 10, 11, IC Y.

Measure pulses at the "Data Bus Buffered".
(Pin 7 to Pin 14 St A).

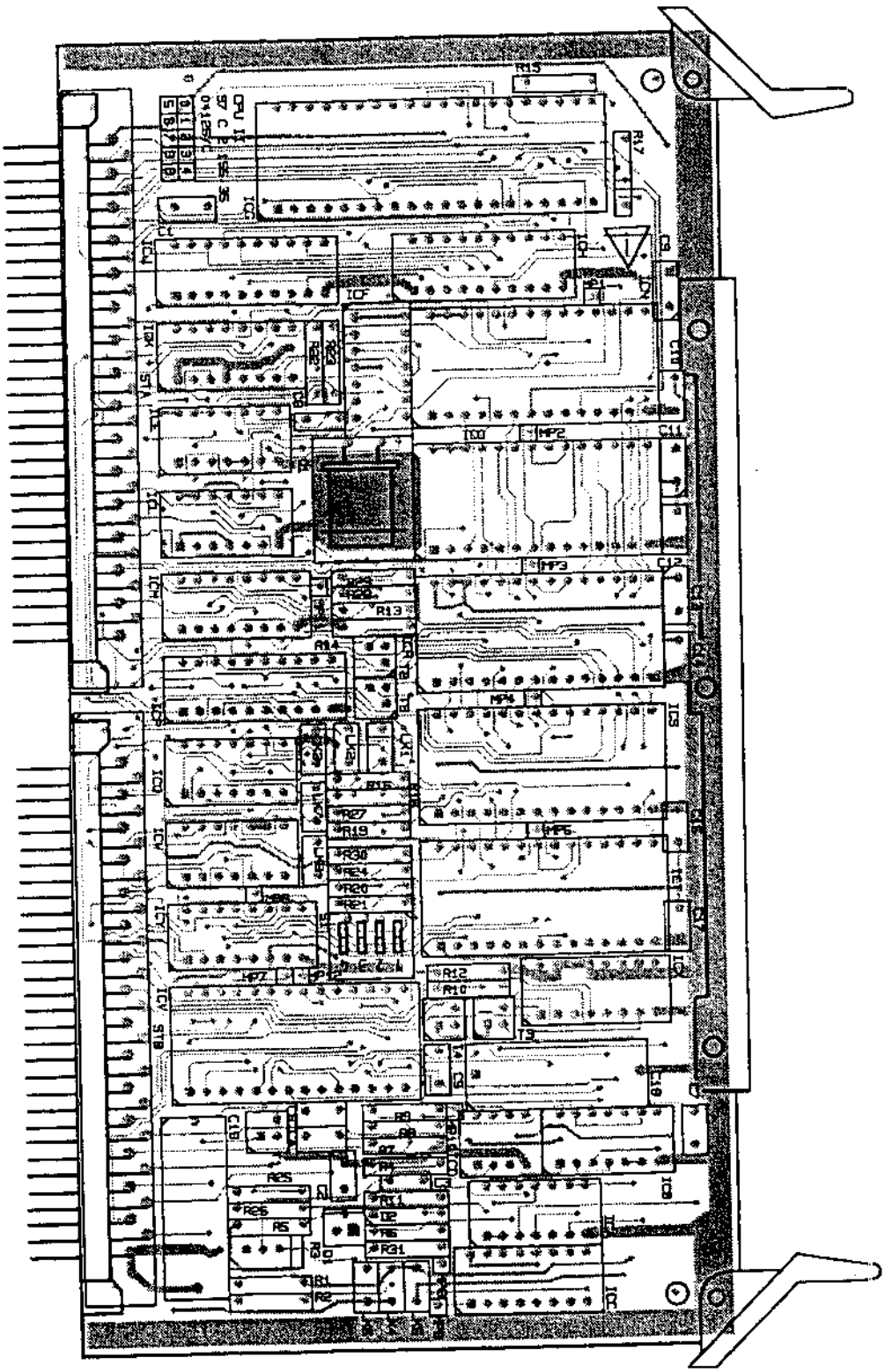
-CPU II-

Measure TXD pulses (Pin 4 socket B).
Measure pulses at IORQ (Pin 23 socket B).
Measure pulses at WR (Pin 24 socket B).
Measure pulses at RD (Pin 25 socket B).
Measure pulses at Φ (Pin 26 socket B).
(Φ timing = symmetrical square wave of 2.5 MHz)

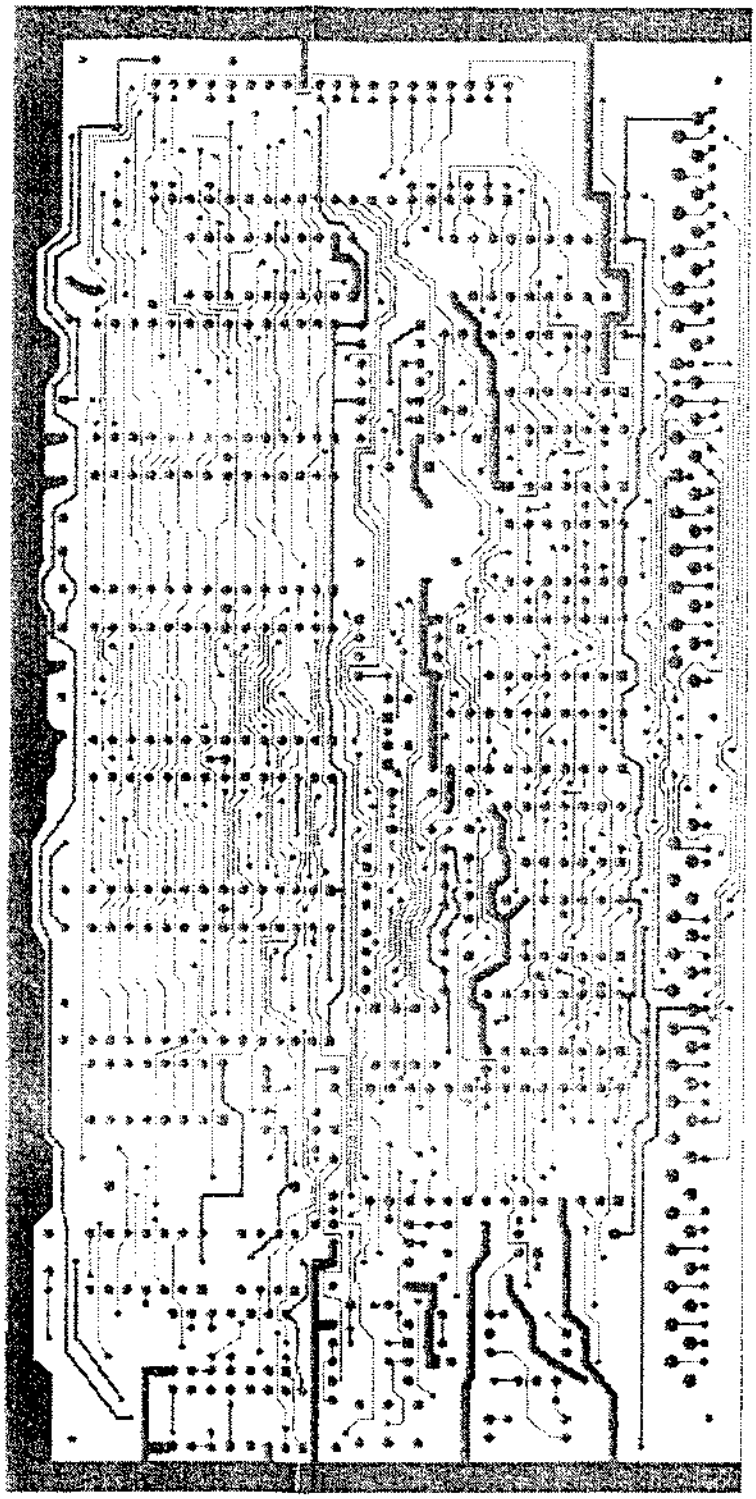
Measure pulses at M1 (Pin 28 socket B).
Measure pulses at MRQ (Pin 29 socket B).
Measure pulses at Address Bus (Pin 15 to 30 socket A).

Remove test EPROM, insert "normal" EPROM set, insert board in a test receiver and test all functions.

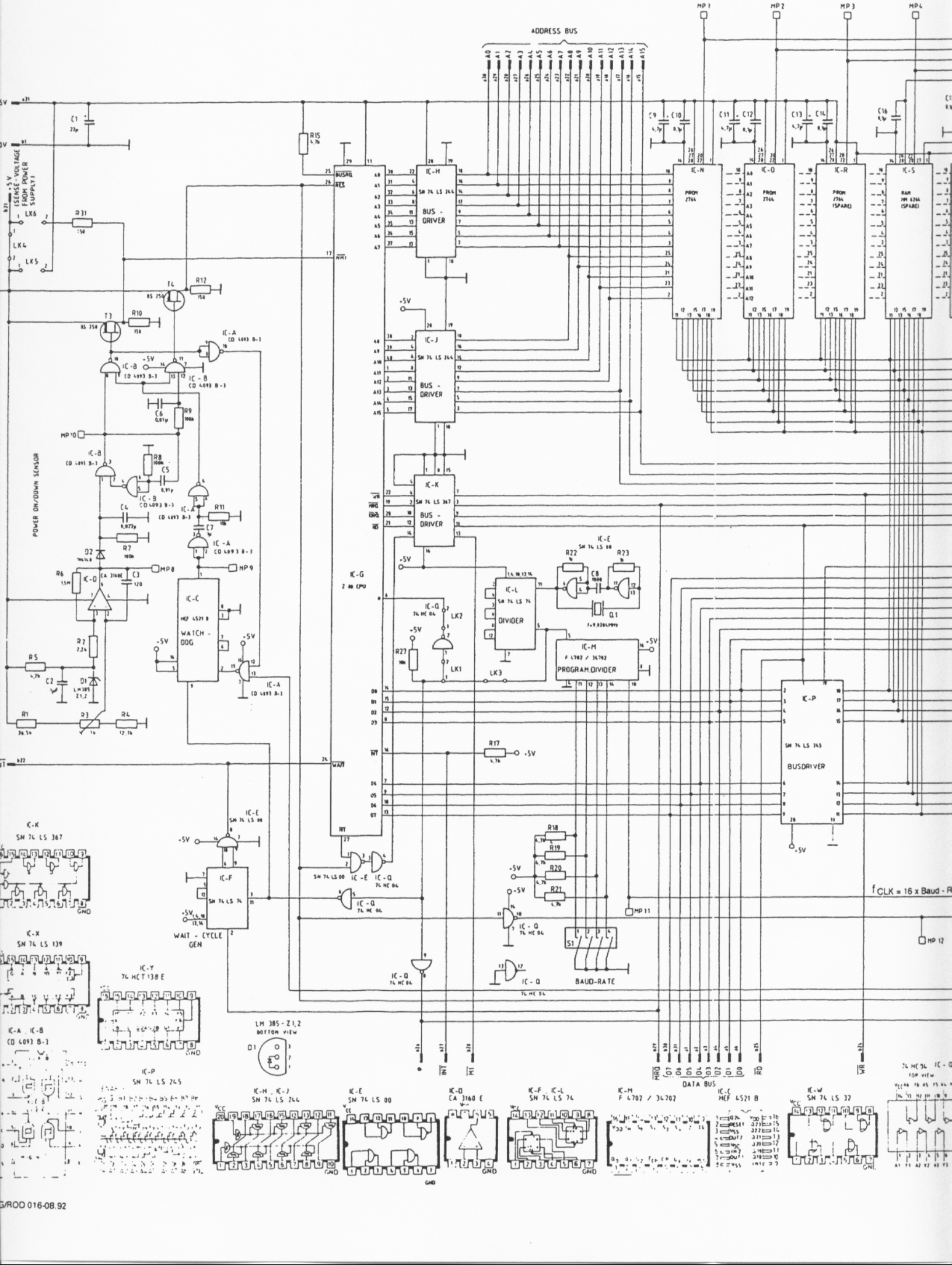
see

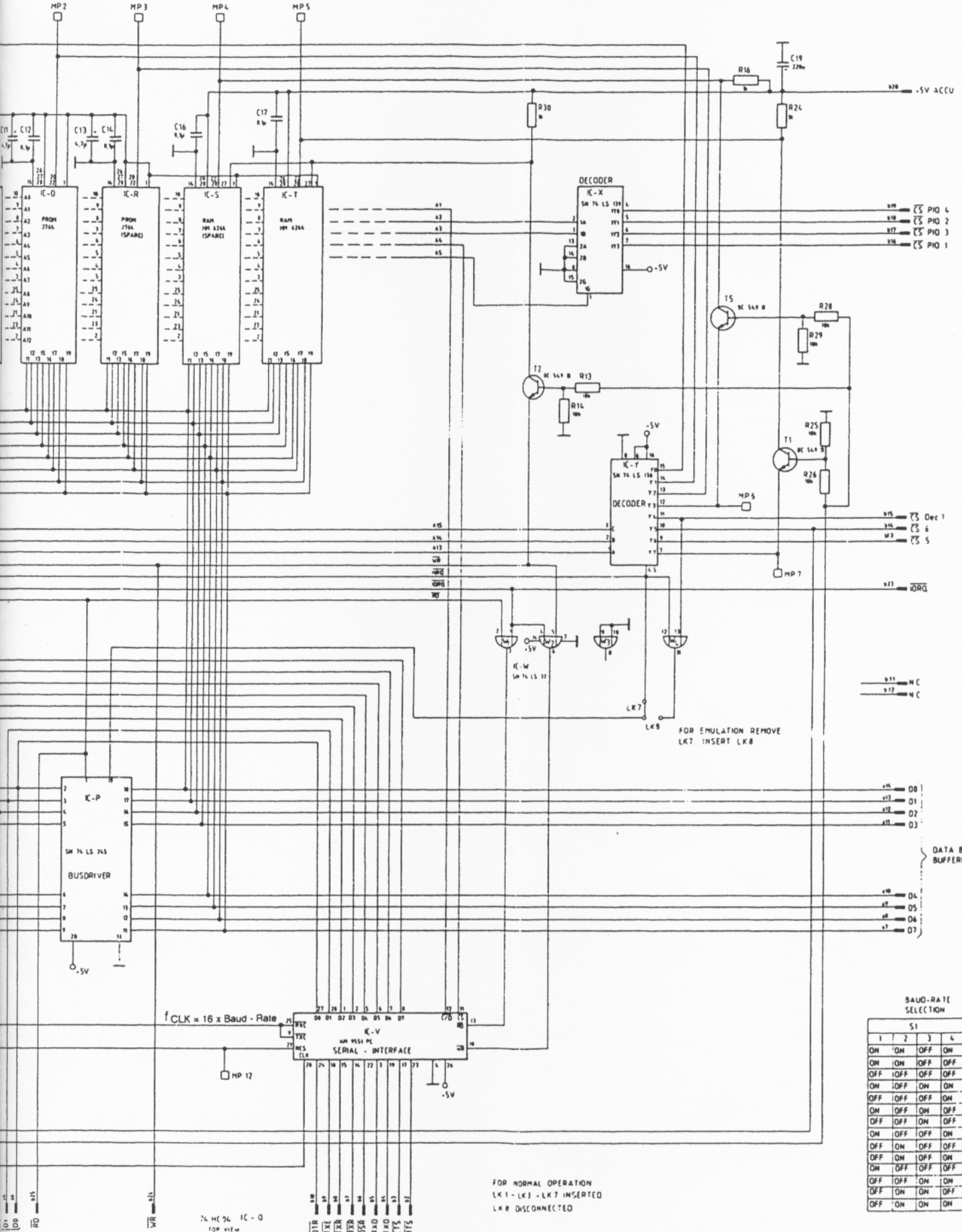


see circuit diagram - 97 Sa B 2.155.35



Printed Circuit Board
CPU II
97 C 2.155.35


ADDRESS BUS
MP 1
MP 2
MP 3
MP 4
IC-H
BUS - DRIVER
IC-J
BUS - DRIVER
IC-K
BUS - DRIVER
IC-N
PROM 2764
IC-O
PROM 2764
IC-R
PROM 2764 (SPARE)
IC-S
RAM HM 6264 (SPARE)
IC-G
Z 80 CPU
IC-C
WATCH - DOG
IC-L
DIVIDER
IC-M
PROGRAM DIVIDER
IC-P
BUSDRIVER
IC-E
IC-F
WAIT - CYCLE GEN
S1
BAUD-RATE
POWER ON/DOWN SENSOR
DATA BUS
fCLK = 16 x Baud - R
IC-K
SN 74 LS 367
IC-X
SN 74 LS 139
IC-Y
74 HCT 138 E
IC-A , IC-B
CD 4093 B-3
IC-P
SN 74 LS 245
LM 385 - Z1,2
BOTTOM VIEW
IC-H , IC-J
SN 74 LS 244
IC-E
SN 74 LS 00
IC-O
CA 3160 E
IC-F , IC-L
SN 74 LS 74
IC-M
F 4702 / 34702
IC-E
HEF 4521 B
IC-W
SN 74 LS 32
G/ROD 016-08.92



BAUD-RATE SELECTION

S1				BAUD-RATE
1	2	3	4	Bd
ON	ON	OFF	ON	50
ON	ON	OFF	OFF	75
OFF	OFF	OFF	OFF	110
ON	OFF	ON	ON	134.5
OFF	OFF	OFF	ON	150
ON	OFF	ON	OFF	200
OFF	OFF	ON	OFF	300
ON	OFF	OFF	ON	600
OFF	ON	OFF	OFF	1200
OFF	ON	OFF	ON	1800
ON	OFF	OFF	OFF	2400
OFF	OFF	ON	ON	2400
OFF	ON	ON	OFF	4800
OFF	ON	ON	ON	9600

CPU II
Circuit Diagram
97 Sa B 2.155.35

Ident-N0.	Mark	Electr. value	Identity	Manufacturer
Capacitors:				
1401.343	C1	22/20/10 V	2222 122 54229	VALVO
1469.053	C2	1/10/50 V	MKS 2 RM 5	WIMA
1304.291	C3	120 pF/2/63 V	NPO-1 B EDPU DIN 41923	
1672.835	C4	0,022l/5/63 V	MKS 2 RM 5	WIMA
1811.541	C5	0,01/10/63 V	MKS 2	WIMA
1811.541	C6	0,01/10/63 V	MKS 2	WIMA
1469.053	C7	1/10/50 V	MKS 2 RM 5	WIMA
1116.282	C8	1000 PF/20/200 V	CK 05 BX 102 M	SEC
1390.376	C9	4,7/20/10 V	2222 122 54478	VALVO
1423.037	C10	0,1/20/63 V	MKS 2	WIMA
1390.376	C11	4,7/20/10 V	2222 122 54478	VALVO
1423.037	C12	0,1/20/63 V	MKS 2	WIMA
1390.376	C13	4,7/20/10 V	2222 122 54478	VALVO
1423.037	C14	0,1/20/63 V	MKS 2	WIMA
1423.037	C16	0,1/20/63 V	MKS 2	WIMA
1423.037	C17	0,1/20/63 V	MKS 2	WIMA
1183.389	C18	220/50/10/10 V	B41283-C3227-T	SIEMENS
1183.289	C19	220/50/10/10 V	B41283-C3227-T	SIEMENS
Diodes:				
1469.983	D1		LM 385 Z 1,2	NATIONAL
0745.677	D2		1 N 4148	
Resistors:				
1405.381	R1	36,5 k-1-50-0207	DIN 44061-G	
0744.808	R2	2,2 k-5-0,6-0207	DIN 44052	
1539.191	R3	1 k/10/0,5 W	752-208	VITROHM
1491.423	R4	12,1 k-1-50-0207	DIN 44061-G	
0767.212	R5	4,7 k-5-0,6-0207	DIN 44052-G	
0933.716	R6	1,5 M-5-0,6-0207	DIN 44052-G	
0767.190	R7	100 k-5-0,6-0207	DIN 44052-G	
0767.190	R8	100 k-5-0,6-0207	DIN 44052-G	
0767.190	R9	100 k-5-0,6-0207	DIN 44052-G	
0744.743	R10	150-5-0,6-0207	DIN 44052-G	
0179.701	R11	10 k-5-0,6-0207	DIN 44052-G	
0744.743	R12	150-5-0,6-0207	DIN 44052-G	
0179.701	R13	10 k-5-0,6-0207	DIN 44052-G	
0179.701	R14	10 k-5-0,6-0207	DIN 44052-G	

Ident-No.	Mark	Electr. value	Identity	Manufacturer
0767.212	R15	4,7 k-5-0,6-0207	DIN 44052-G	
0179.698	R16	1 k-5-0,6-0207	DIN 44052-G	
0767.212	R17	4,7 k-5-0,6-0207	DIN 44052-G	
0767.212	R18	4,7 k-5-0,6-0207	DIN 44052-G	
0767.212	R19	4,7 k-5-0,6-0207	DIN 44052-G	
0767.212	R20	4,7 k-5-0,6-0207	DIN 44052-G	
0767.212	R21	4,7 k-5-0,6-0207	DIN 44052-G	
0179.698	R22	1 k-5-0,6-0207	DIN 44052-G	
0179.698	R23	1 k-5-0,6-0207	DIN 44052-G	
0179.698	R24	1 k-5-0,6-0207	DIN 44052-G	
0179.701	R25	10 k-5-0,6-0207	DIN 44052-G	
0179.701	R26	10 k-5-0,6-0207	DIN 44052-G	
0179.701	R27	10 k-5-0,6-0207	DIN 44052-G	
0179.701	R28	10 k-5-0,6-0207	DIN 44052-G	
0179.701	R29	10 k-5-0,6-0207	DIN 44052-G	
0179.701	R30	10 k-5-0,6-0207	DIN 44052-G	
0744.743	R31	150-5-0,6-0207	DIN 44052-G	

Integrated circuits:

1331.876	IC A		CD 4093 B	RCA, NATIONAL
1331.876	IC B		CD 4093 B	RCA, NATIONAL
1398.326	IC C		HEF 4521 BP	VALVO
	IC D		CA 3160 E	RCA
1090.895	IC E		ND 74 LS 00 N	
1186.787	IC F		SN 74 LS 74	TEXAS
			DM 74 LS 74 AN	NATIONAL
1911.244	IC G	IC Z 84 C00 AB6 Z 80 CPU, C-MOS, 4 MHz		SGS
1398.296	IC H		74 LS 244 N	
1398.296	IC J		74 LS 244 N	
1398.490	IC K		74 LS 376 N	NS, TEXAS
1186.787	IC L		SN 74 LS 74	TEXAS
			DM 74 LS 74 AN	NATIONAL
1776.029	IC M		F 4702 BPC	
1865.595	IC N			97 E 2.155.260
1865.595	IC O			97 E 2.155.260
1486.756	IC P		74 LS 245	NATIONAL, VALVO, TEXAS, MOTOROLA
	IC Q		74 HC 04	NATIONAL
1713.167	IC T		HM 6264 LP - 15	HITACHI
1478.877	IC V		AM 9551 PC	AMD

HAG/ROD 016-09 92

-CPU II-

Ident-No.	Mark	Electr. value	Identity	Manufacturer
1398.563	IC W		74 LS 32 N	NS, TEXAS
1425.080	IC X		SN 74 LS 139 N	NS, TEXAS, FAIRCHILD
	IC Y		74 HCT 138 E	

Transistors:

1291.033	T1		BC 549 B	ROE, INTERMET, VALVO
1291.033	T2		BC 549 B	ROE, INTERMET, VALVO
1465.767	T3		BS 250	ITT
1465.767	T4		BS 250	ITT
1291.033	T5		BC 549 B	ROE, INTERMET, VALVO

Supplements:

1404.229	Q1	9.8304 MHz	HC-18/U	
1315.293	S1	4-quad	435166-2	AMP
0681.296	ST A		DIN 41617	
0681.296	ST B		DIN 41617	